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06CS81

Eighth Semester B.E. Degree Examination, Dec.2013/Jan.2014
Advanced Computer Architectures

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define Instruction Set Architecture (ISA). Explain seven dimensions of an ISA. **(08 Marks)**

b. Find the number of dies per 500 mm wafer for a die that is 2.0 cm on a side. **(04 Marks)**

c. Explain main measures of dependability. **(04 Marks)**

d. Derive CPU time in term of instruction cycle and cycles per instruction. **(04 Marks)**

2 a. Explain basics of a RISC instruction set. **(05 Marks)**

b. Show with diagram, how data hazard stalls are minimized by forwarding method. **(07 Marks)**

c. List the type of exceptions. Explain requirements on exceptions. **(08 Marks)**

3 a. Define ILP. Explain data dependencies and hazards in detail. **(08 Marks)**

b. With finite state processor, explain 2-bit prediction scheme. **(05 Marks)**

c. Explain hardware-based speculation with steps involved in instruction execution. **(07 Marks)**

4 a. What are the three major flavours of multiple issue processor? Summarize the basic approaches to multiple issue and their distinguishing characteristics. **(08 Marks)**

b. Explain branch target buffer with neat diagrams. **(06 Marks)**

c. What are the issues involved in implementation of speculation? Explain register renaming approach. **(06 Marks)**

PART – B

5 a. Explain taxonomy of parallel architecture according to Flynn. **(06 Marks)**

b. To achieve a speedup of 80 with 100 processors, what fraction of the original computation can be sequential? **(06 Marks)**

c. Explain the basic of directory based cache coherence protocol. **(08 Marks)**

6 a. Assume a computer where the clocks per instruction is 1.0 when all memory accesses hit in the cache. Only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instruction were cache hits? **(06 Marks)**

b. Explain following cache optimizations:
i) Higher associativity to reduce miss rate
ii) Read misses over writes to reduce miss penalty. **(08 Marks)**

c. Explain techniques for fast address translation. **(06 Marks)**

7 a. Explain "compiler optimizations to reduce miss rate" in advanced cache optimization. **(08 Marks)**

b. Explain DRAM memory technology with its basic organization. **(08 Marks)**

c. Write a note on protection via virtual machines. **(04 Marks)**

8 a. Explain loop level dependencies by considering following code:

```
for (i = 1; i <=100; i = i + 1) {
A[i] = A[i] + B[i];
B[i] = C[i] + D[i]; }
```

(06 Marks)

b. Explain software pipelining with symbolic loop unrolling. **(09 Marks)**

c. List and explain five execution unit slots in the IA-64 architecture with example instructions. **(05 Marks)**

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